IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claim 1 (Currently Amended): A semiconductor device comprising:

a semiconductor substrate having a main surface along which a semiconductor element is formed;

interlayer insulating films formed on said main surface;

conductive interconnections provided in a plurality of layers separated by said interlayer insulating films;

conductive dummy interconnections provided in the plurality of layers so that every one of said conductive dummy interconnections is formed in a layer of said plurality of layers with at least one conductive interconnection; and

a conductive dummy plug selectively buried in said interlayer insulating films to connect said dummy interconnections between said two or more layers and connected together with said dummy interconnections to a stable potential line which is included in said interconnections and which holds a constant potential with respect to a potential carried on a lower-potential power-supply line or a higher-potential power-supply line,

wherein said dummy interconnections are provided to sandwich an interconnection part included in said interconnections in at least one layer of said plurality of layers, and

wherein said dummy interconnections also comprise a dummy interconnection which is provided in a layer located over said at least one layer to cover said interconnection part.

Claims 2-8 (Canceled).

Claim 9 (Original): The semiconductor device according to claim 1, wherein said stable potential line is any of said lower-potential power-supply line, said higher-potential power-supply line, a precharge line included in said interconnections and carrying a precharge potential, and a substrate potential line included in said interconnections and carrying a substrate potential.

Claim 10 (Previously Presented): A semiconductor device comprising:

a semiconductor substrate having a main surface along which a semiconductor element is formed;

interlayer insulating films formed on said main surface;

conductive interconnections provided in a plurality of layers separated by said interlayer insulating films; and

conductive dummy interconnections provided in the same layers as said interconnections in two or more layers included in said plurality of layers,

wherein at least one of said dummy interconnections has repetitive protrusions and recesses along its elongate direction in a section taken along said main surface.

Claim 11 (Previously Presented): A semiconductor device comprising:

a semiconductor substrate having a main surface along which a semiconductor element is formed;

interlayer insulating films formed on said main surface;

conductive interconnections provided in a plurality of layers separated by said interlayer insulating films; and

conductive dummy interconnections provided in the same layers as said interconnections in two or more layers included in said plurality of layers,

wherein at least one of said dummy interconnections has repetitive protrusions and recesses along its elongate direction in a section taken along a plane perpendicular to said main surface.

Claim 12 (Original): The semiconductor device according to claim 11, wherein the protrusions among said repetitive protrusions and recesses are connected to a part of said dummy interconnection provided in a lower layer.

Claim 13 (Original): The semiconductor device according to claim 1, further comprising a passivation film converting the uppermost layer among said plurality of layers and having a higher thermal conductivity than said interlayer insulating films.

Claim 14 (Original): The semiconductor device according to claim 13, further comprising a heat sink which is in contact with said passivation film.

Claim 15 (Original): The semiconductor device according to claim 14, wherein said dummy interconnections also comprise one which is provided in said uppermost layer, and

said semiconductor device further comprises another conductive dummy plug selectively buried in said passivation film to connect said heat sink and part of said dummy interconnection which belongs to said uppermost layer.

Claims 16-20 (Canceled).

Claim 21 (Previously Presented): The semiconductor device according to claim 10, wherein potentials corresponding to each of said lower-potential power-supply line or a higher-potential power-supply line are connected to said dummy conductive plug

Claim 22 (Previously Presented): The semiconductor device according to claim 10, comprising:

a conductive dummy plug selectively buried in said interlayer insulating films to connect said dummy interconnections between said two or more layers and connected together with said dummy interconnections to a stable potential line which is included in said interconnections and which holds a constant potential with respect to a potential carried on a lower-potential power-supply line or a higher-potential power-supply line.

Claim 23 (Previously Presented): The semiconductor device according to claim 11, comprising:

a conductive dummy plug selectively buried in said interlayer insulating films to connect said dummy interconnections between said two or more layers and connected together with said dummy interconnections to a stable potential line which is included in said interconnections and which holds a constant potential with respect to a potential carried on a lower-potential power-supply line or a higher-potential power-supply line.